oxide, having a thickness of approximately 2 nm, a first metal layer **230**B (e.g., a layer of titanium nitride with a thickness of about 1-2 nm), a second metal layer **230**C (e.g., a layer of tantalum nitride with a thickness of about 1-2 nm), a third metal layer **230**D (e.g., a layer of titanium nitride with a thickness of about 5 nm) and a bulk metal layer **230**E, such as aluminum. Ultimately, as shown in FIG. **1**D, one or more CMP processes are performed to remove excess portions of the gate insulation layer **230**A, the first metal layer **230**B, the second metal layer **230**C, the third metal layer **230**D and the bulk metal layer **230**E positioned outside of the gate cavity **220** to thereby define the replacement gate structure **230**.

[0010] As device dimensions have decreased and packing densities have increased, parasitic capacitance is becoming more important as a factor to consider to improve the operating speed of transistor devices. Typically, as noted above, the gate structure of a transistor will include at least one sidewall spacer positioned adjacent the gate structure. Typically, the sidewall spacers are made of silicon nitride and they are normally formed very soon after the final gate structure is formed using a "gate-first" manufacturing technique or after the sacrificial gate structure is formed for devices manufactured using the replacement gate technique. One of the primary purposes of the silicon nitride spacers for "gate-first" devices is to protect the gate materials during subsequent processing operations. For "replacement gate" devices, the spacers also serve to protect the replacement gate structure and to define the gate cavity in the replacement gate manufacturing process.

[0011] Unfortunately, the k-value of silicon nitride is relatively high, e.g., about 7-8. The presence of the silicon nitride spacer material (with a relatively high k-value) tends to increase the parasitic capacitance between the conductive gate electrode and conductive contacts (like trench silicide regions) that are formed in close proximity to the gate structure of the transistor. This problem has become even more problematic as packing densities have increased which causes the gate structures of adjacent transistor to be positioned ever closer to one another. The use of so-called self-aligned contacts has also exacerbated this problem.

[0012] The use of alternative materials for the sidewall spacers, such as materials having k values less than about 6 or so, has been problematic. Most of such low-k materials are based upon carbon or boron doped silicon nitride. The low-k material, when used as a traditional spacer material, is subjected to a reactive ion etching (RIE) process to define the spacer from such a low-k material. The RIE process tends to deplete the carbon and boron, thereby effectively increasing the k-value of the low-k material. Such low-k materials also tend to be weaker mechanically than silicon nitride, which makes them less capable of standing up to the rigors of processing after they are formed. Moreover, such spacers are typically subjected to relatively high temperature source/drain anneal processes, which also tends to deplete the carbon and boron from such low-k materials.

[0013] The present disclosure is directed to various methods of forming a semiconductor device with low-k spacers and various semiconductor devices incorporating such low-k spacers that may solve or reduce one or more of the problems identified above.

SUMMARY OF THE INVENTION

[0014] The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

[0015] Generally, the present disclosure is directed to various methods of forming a semiconductor device with low-k spacers and various semiconductor devices incorporating such low-k spacers. One illustrative method disclosed herein includes forming a sacrificial gate structure above a semiconducting substrate, forming at least one sacrificial sidewall spacer adjacent the sacrificial gate structure, removing at least a portion of the sacrificial gate structure to thereby define a gate cavity that is laterally defined by the sacrificial sidewall spacer, forming a replacement gate structure in the gate cavity, after forming the replacement gate structure, removing the sacrificial sidewall spacer to thereby define a spacer cavity adjacent the replacement gate structure, and forming a low-k spacer in the spacer cavity.

[0016] Another illustrative method includes forming a sacrificial gate structure above a semiconducting substrate, forming a first sacrificial sidewall spacer adjacent the sacrificial gate structure, forming a second sacrificial sidewall spacer adjacent the first sacrificial sidewall spacer and performing a first etching process to remove the second sacrificial sidewall spacer relative to the first sacrificial sidewall spacer to thereby define a first spacer cavity. In this embodiment, the method further includes the steps of forming a third sacrificial sidewall spacer in the first spacer cavity adjacent the first sacrificial sidewall spacer, after forming the third sacrificial sidewall spacer, removing at least a portion of the sacrificial gate structure to thereby define a gate cavity that is laterally defined by the first sacrificial sidewall spacer, forming a replacement gate structure in the gate cavity, after forming the replacement gate structure, removing at least the first and third sacrificial sidewall spacers to thereby define a second spacer cavity adjacent the replacement gate structure, and forming a low-k spacer in the second spacer cavity.

[0017] One example of a novel device disclosed herein includes a gate structure positioned above a semiconducting substrate, wherein the gate structure includes a gate insulation layer and a gate electrode. In this example, the gate insulation layer has two upstanding portions that are substantially vertically oriented relative to an upper surface of the substrate. The device further includes a low-k sidewall spacer positioned adjacent each of the vertically oriented upstanding portions of the gate insulation layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

[0019] FIGS. **1**A-**1**D depict one illustrative prior art process flow for forming a semiconductor device using a so-called "gate last" or "replacement gate" approach; and

[0020] FIGS. **2**A-**2**Q depict one illustrative method disclosed herein for forming an illustrative semiconductor device with low-k spacers.

[0021] While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be